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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,277	09/21/2000	David William Boerstler	AUS9-2000-0240-US1	8443

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EXAMINER	
PATHAK, SUDHANSHU C	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/666,277	BOERSTLER, DAVID WILLIAM	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 12th, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,28-35,37,38,47 and 50* is/are rejected.

7)☒ Claim(s) *13-27,36,39-46,48 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *September 21st, 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-50 are pending in the application.

2. In view of the appeal brief filed on October 12th, 2004, **PROSECUTION IS HEREBY REOPENED**, as set forth below.

   To avoid abandonment of the application, appellant must exercise one of the following two options:

   (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

   (2) request reinstatement of the appeal.

   If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 29-34 & 50 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. The Claim is vague because it recites functional language not supported by recitation in the claim of sufficient structure to warrant the presence of the functional language in the claim.

Regarding to Claims 29-34 & 50, the claims refer to "inputting the compared output signal at a second flip-flop circuit component", however the claim does not disclose a "first flip-flop", it is not clear how the first flip-flop is implemented in the clock recovery circuit.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9 & 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Dobias (3,967,061).

Regarding to Claims 1-9 & 28, Dobias discloses method and apparatus for recovering data and clock information in a self-clocking data stream (Abstract, lines 1-3 & Column 1, lines 5-15, 58-66 & Fig. 's 1, 3, 4). Dobias discloses the method comprising the steps of: inputting a received data signal to both a first monostable circuit component and a second monostable circuit component and generating a first output signal from the first monostable circuit component and a second output signal from the second monostable circuit component (Fig. 3, elements 15, 16, 21, 23-24, 25-26, 28 & Abstract, lines 3-6 & Column 2, lines 6-16 & Column 3, lines 35-68 & Column 4, lines 1-21 & Claim 20); comparing the first output signal and the second output signal to each other using a first logical operator and outputting a compared output signal based on the comparison (Fig. 3, elements 30, 17, 19, 31-32 & Column

2, lines 13-20 & Column 3, lines 60-68 & Column 4, lines 20-25). Dobias also discloses the signal clock recovery consisting of at least one of a clock signal and a data signal (Fig.'s 1, 3-5 & Column 2, lines 40-51 & Column 4, lines 8-60 & Column 5, lines 8-68). Dobias also discloses the first logical operator to be an OR-gate logical operator (Fig. 3, element 30 & Column 2, lines 17-18, 26-30 & Column 4, lines 8-9, 22-23). Dobias also discloses the compared output signal is a recovered clock output signal (Fig. 3, elements 30, 17, 19, 31-32 & Column 4, lines 22-61). Dobias also discloses that at least one of the first monostable circuit component and the second monostable circuit component are one-shot circuit components (Column 3, lines 35-60 & Column 4, lines 8-22). Dobias also discloses that the first and second generated output signals are at least one of a ones clock output signal and a zeros clock output signal (Fig. 3, elements 16, 16, 21, 23-24, 25-26 & Column 3, lines 35-66).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 10-11, 35, 37-38 & 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobias (3,967,061) in view of Park (5,880,898).

Regarding to Claims 10-11, 35, 37-38 & 47, Dobias discloses method and apparatus for recovering data and clock information in a self-clocking data stream

comprising a first and second monostable circuits and comparing the outputs of the monostable circuits using a first logical operator as described above. However, Dobias does not disclose an equalizer to equalize the received input data signal.

Park discloses a circuit to equalize or remove error signals in digital data signals (Abstract, lines 6-11). Park discloses the equalizer circuit (Fig. 3, element 100 & Figure 4) to include a differentiator (Fig. 4, element 61) for differentiating the input signal, an amplifier (Fig. 4, elements 62 & 63) for amplifying the differentiated data, a sign element (Fig. 4, element 70) to apply a sign to the amplified data. The signed amplified data signal is decreased due to the attenuation and coupling of the signals in the transmission lines. Park discloses a circuit to equalize or remove error signals in digital data signals (Abstract, lines 6-11). Park further discloses the equalizer comprising at least one output port (Fig. 3, element 100 & Fig. 4, element "NON-GLITCH"). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the equalizer as described in Park to the clock recovery circuit as described in Dobias so as to remove any glitches or distortions in the received data so as to accurately then recover the clock and decode the data signals.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dobias (3,967,061) in view of Park (5,880,898) in further view of Streckmann et al. (4,535,299).

Regarding to Claim 12, Dobias in view of Park discloses method and apparatus for recovering data and clock information in a self-clocking data stream comprising a

first and second monostable circuits and comparing the outputs of the monostable circuits using a first logical operator and an equalizer to equalize the received input data signal as described above. Park further discloses that an optimum differentiation width can be set by varying the time constant to remove a glitch than the data (Column 4, lines 12-15). However Dobias in view of Park does not disclose the differentiator to as a resistive-capacitive differentiator.

Streckmann discloses a resistive-capacitive differentiator (Fig. 1, elements C1 & R1), for differentiating the incoming signal (Column 3, lines 57-63). Furthermore, Streckmann discloses varying the values of the resistor and /or the capacitor so as to obtain the optimum time constant for the frequency of the incoming signal (Column 3, lines 57-67 & Column 4, lines 15-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by implementing the differentiator as described in Streckmann in the clock recovery circuit and decoder as described in Dobias in view of Park the optimum time constant can be achieved by varying the R-C values of the differentiator, and thus provide increased flexibility for the data rate into the equalizer.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, it is recommended to the applicant to amend all the claims so as to be patentable over the cited prior art of record. A detailed list of pertinent references is included with this Office Action (See Attached "Notice of References Cited" (PTO-892)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

- If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)-272-3056
- The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak

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